



**CY7C1461AV33**  
**CY7C1463AV33**  
**CY7C1465AV33**

## 36-Mbit (1M x 36/2 M x 18/512K x 72) Flow-Through SRAM with NoBL™ Architecture

### Features

- No Bus Latency™ (NoBL™) architecture eliminates dead cycles between write and read cycles
- Supports up to 133-MHz bus operations with zero wait states
  - Data is transferred on every clock
- Pin-compatible and functionally equivalent to ZBT™ devices
- Internally self timed output buffer control to eliminate the need to use OE
- Registered inputs for flow through operation
- Byte Write capability
- 3.3V/2.5V IO power supply
- Fast clock-to-output times
  - 6.5 ns (for 133-MHz device)
- Clock Enable ( $\overline{\text{CEN}}$ ) pin to enable clock and suspend operation
- Synchronous self timed writes
- Asynchronous Output Enable
- CY7C1461AV33, CY7C1463AV33 available in JEDEC-standard Pb-free 100-pin TQFP package, Pb-free and non-Pb-free 165-Ball FBGA package. CY7C1465AV33 available in Pb-free and non-Pb-free 209-Ball FBGA package
- Three chip enables for simple depth expansion
- Automatic Power down feature available using ZZ mode or CE deselect
- IEEE 1149.1 JTAG-Compatible Boundary Scan
- Burst Capability — linear or interleaved burst order
- Low standby power

### Selection Guide

	133 MHz	100 MHz	Unit
Maximum Access Time	6.5	8.5	ns
Maximum Operating Current	310	290	mA
Maximum CMOS Standby Current	120	120	mA

### Functional Description<sup>[1]</sup>

The CY7C1461AV33/CY7C1463AV33/CY7C1465AV33 is a 3.3V, 1M x 36/2M x 18/512K x 72 Synchronous Flow-through Burst SRAM designed specifically to support unlimited true back-to-back Read/Write operations without the insertion of wait states. The CY7C1461AV33/CY7C1463AV33/CY7C1465AV33 is equipped with the advanced No Bus Latency (NoBL) logic required to enable consecutive Read/Write operations with data being transferred on every clock cycle. This feature dramatically improves the throughput of data through the SRAM, especially in systems that require frequent Write-Read transitions.

All synchronous inputs pass through input registers controlled by the rising edge of the clock. The clock input is qualified by the Clock Enable ( $\overline{\text{CEN}}$ ) signal, which when deasserted suspends operation and extends the previous clock cycle. Maximum access delay from the clock rise is 6.5 ns (133-MHz device).

Write operations are controlled by the two or four Byte Write Select ( $\text{BW}_X$ ) and a Write Enable ( $\overline{\text{WE}}$ ) input. All writes are conducted with on-chip synchronous self timed write circuitry.

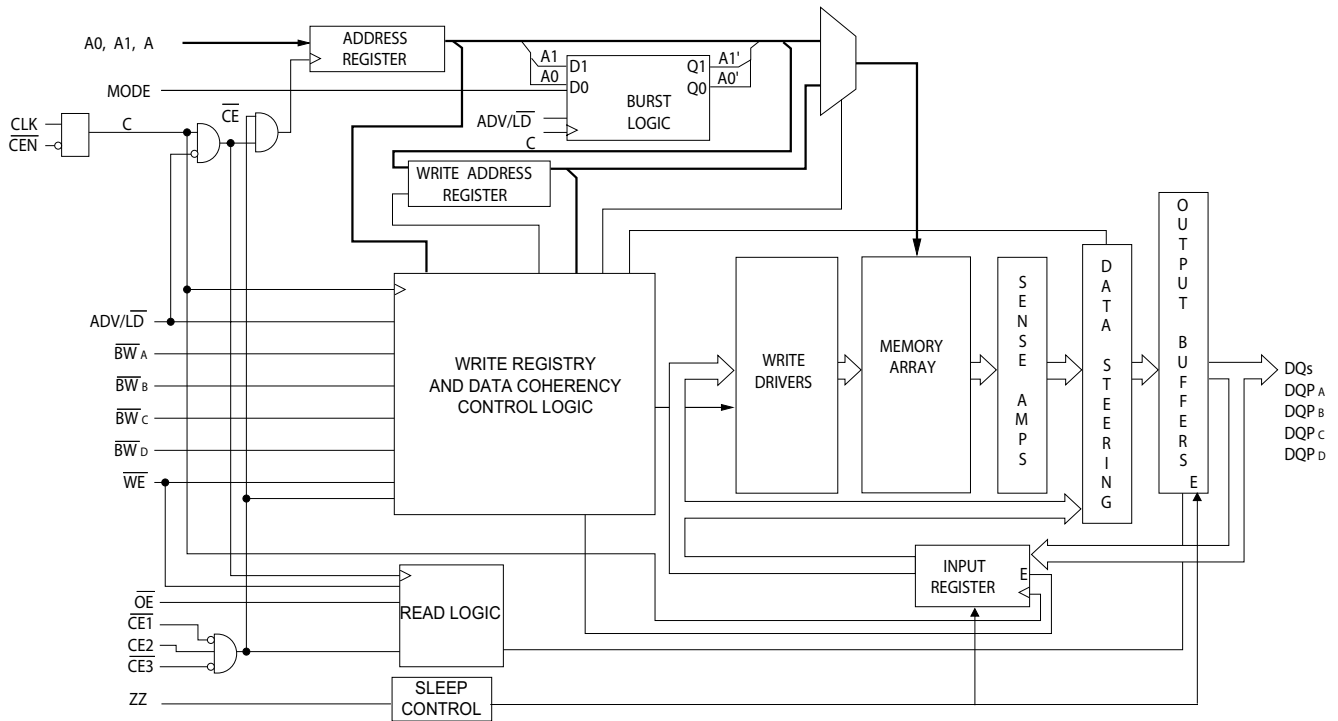
Three synchronous Chip Enables ( $\overline{\text{CE}}_1, \text{CE}_2, \overline{\text{CE}}_3$ ) and an asynchronous Output Enable ( $\text{OE}$ ) provide for easy bank selection and output tri-state control. To avoid bus contention, the output drivers are synchronously tri-stated during the data portion of a write sequence.

#### Note:

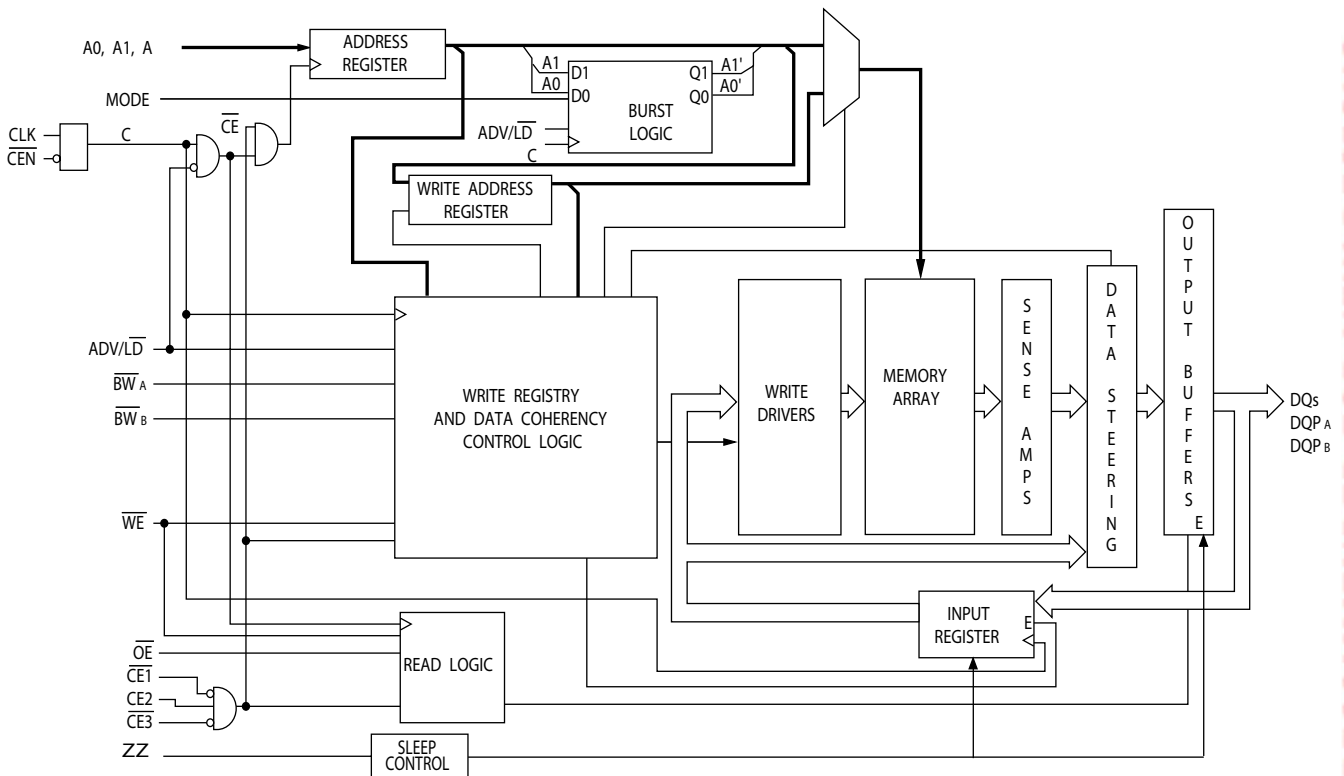
1. For best-practices recommendations, please refer to the Cypress application note *System Design Guidelines* on [www.cypress.com](http://www.cypress.com).

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**Logic Block Diagram – CY7C1461AV33 (1M x 36)**

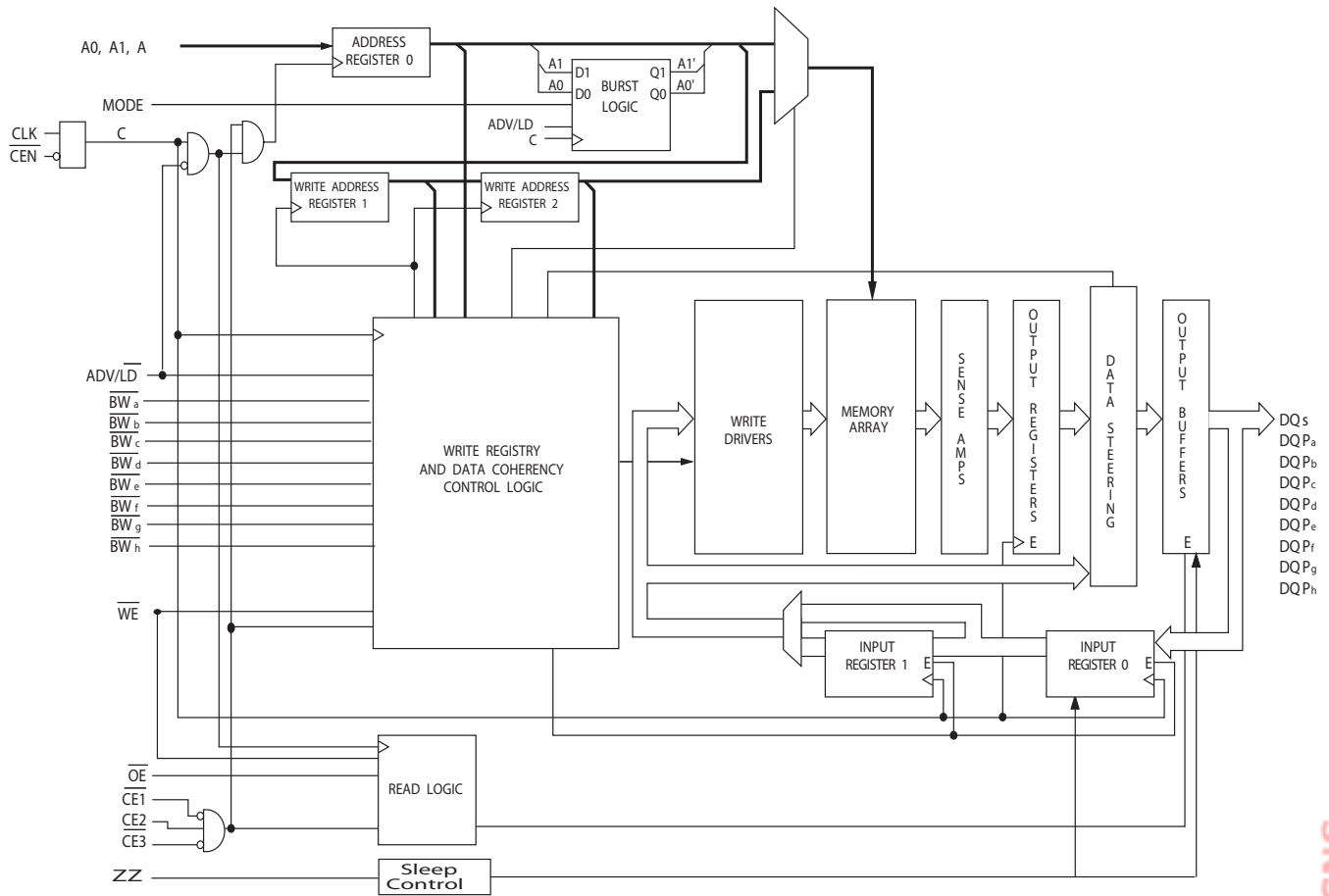


**Logic Block Diagram – CY7C1463AV33 (2M x 18)**



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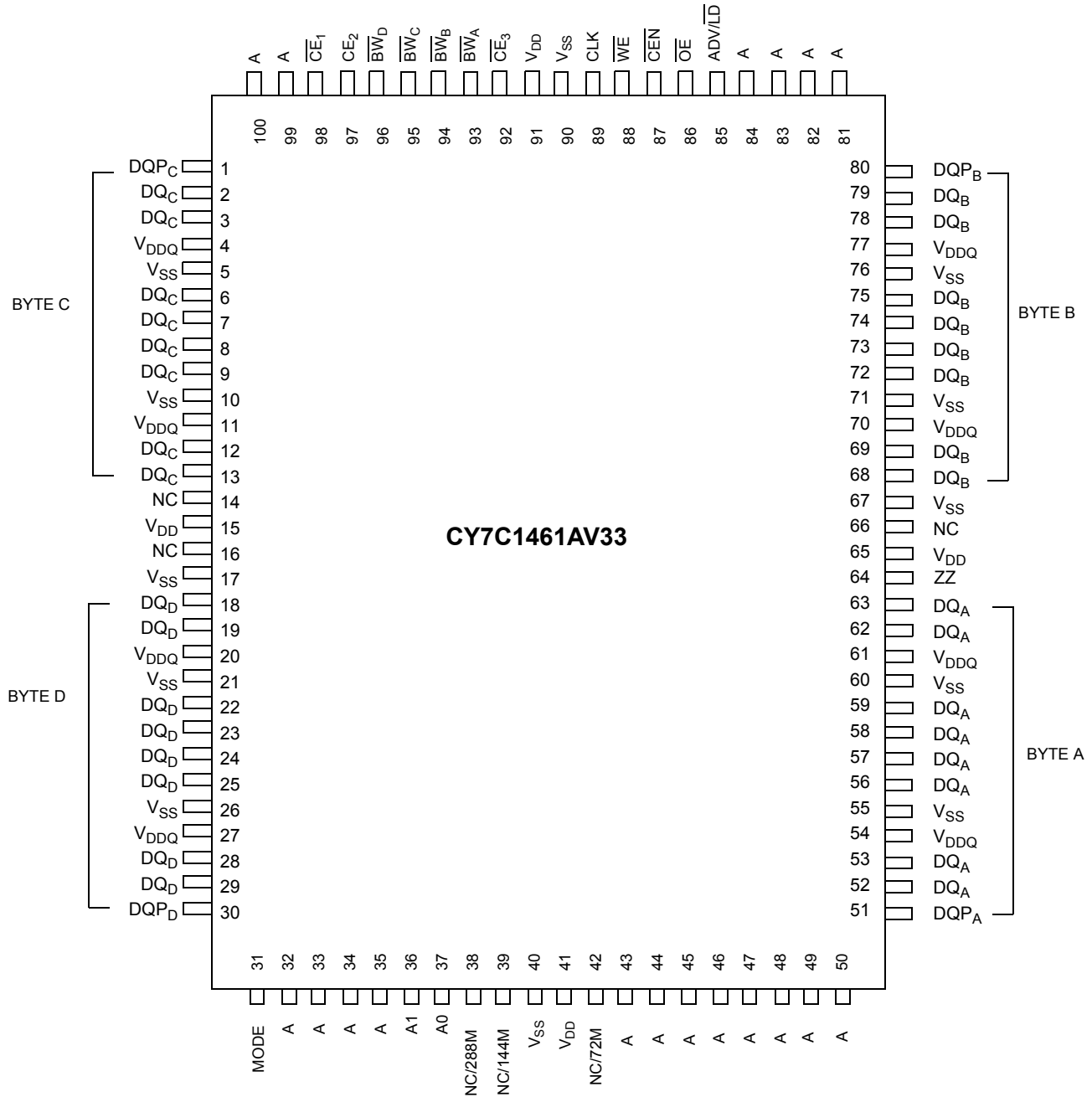
**Logic Block Diagram – CY7C1465AV33 (512K x 72)**



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**Pin Configurations**

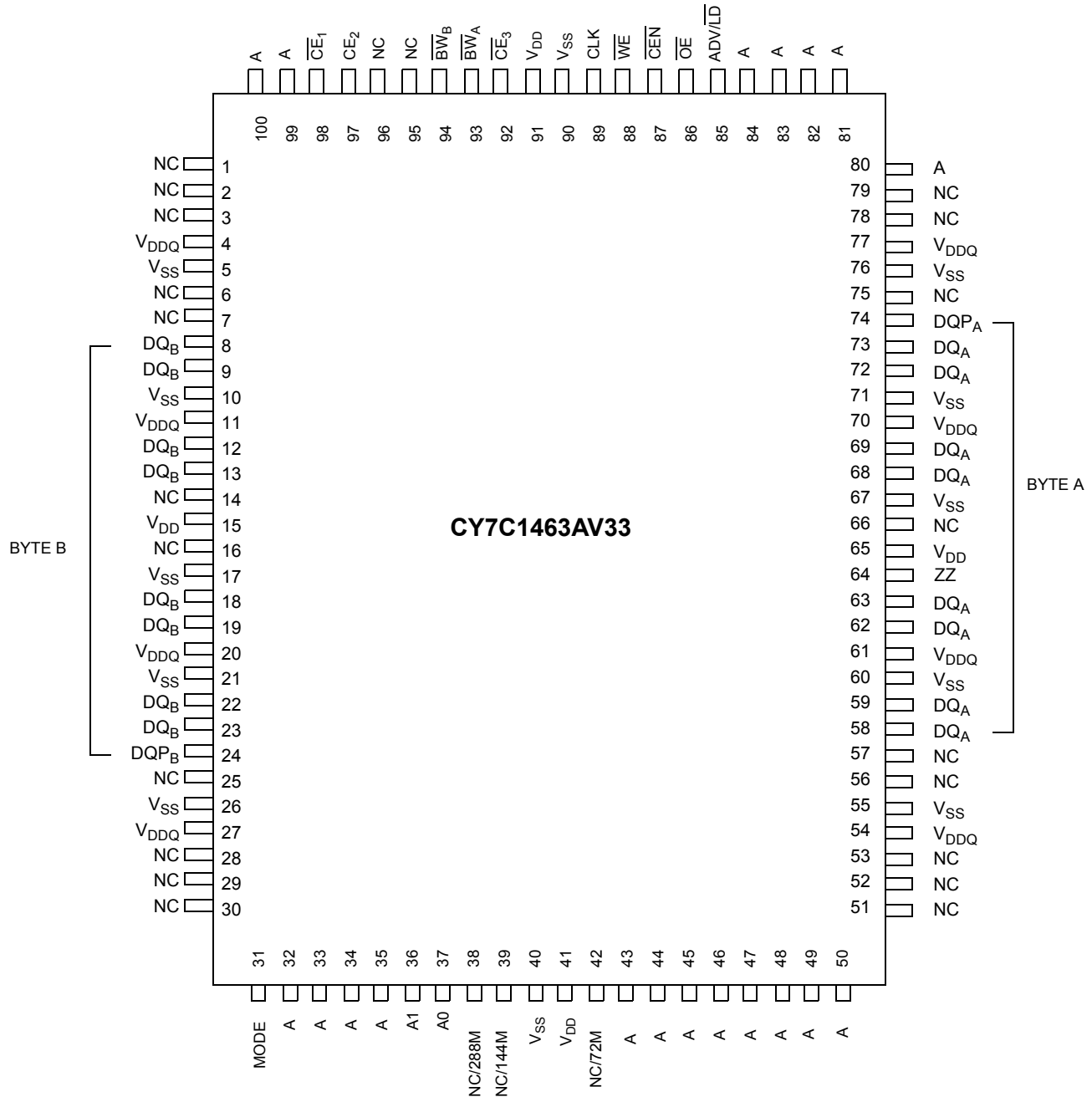
**100-Pin TQFP Pinout**



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**Pin Configurations** (continued)

**100-Pin TQFP Pinout**



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**Pin Configurations** (continued)

**165-Ball FBGA (15 x 17 x 1.4 mm) Pinout**

**CY7C1461AV33 (1M x 36)**

	1	2	3	4	5	6	7	8	9	10	11
<b>A</b>	NC/576M	A	$\overline{CE}_1$	$\overline{BW}_C$	$\overline{BW}_B$	$\overline{CE}_3$	$\overline{CEN}$	ADV/LD	A	A	NC
<b>B</b>	NC/1G	A	CE2	$\overline{BW}_D$	$\overline{BW}_A$	CLK	$\overline{WE}$	$\overline{OE}$	A	A	NC
<b>C</b>	DQ <sub>C</sub>	NC	V <sub>DDQ</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DDQ</sub>	NC	DQP <sub>B</sub>
<b>D</b>	DQ <sub>C</sub>	DQ <sub>C</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQ <sub>B</sub>	DQ <sub>B</sub>
<b>E</b>	DQ <sub>C</sub>	DQ <sub>C</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQ <sub>B</sub>	DQ <sub>B</sub>
<b>F</b>	DQ <sub>C</sub>	DQ <sub>C</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQ <sub>B</sub>	DQ <sub>B</sub>
<b>G</b>	DQ <sub>C</sub>	DQ <sub>C</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQ <sub>B</sub>	DQ <sub>B</sub>
<b>H</b>	NC	NC	NC	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	NC	NC	ZZ
<b>J</b>	DQ <sub>D</sub>	DQ <sub>D</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQ <sub>A</sub>	DQ <sub>A</sub>
<b>K</b>	DQ <sub>D</sub>	DQ <sub>D</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQ <sub>A</sub>	DQ <sub>A</sub>
<b>L</b>	DQ <sub>D</sub>	DQ <sub>D</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQ <sub>A</sub>	DQ <sub>A</sub>
<b>M</b>	DQ <sub>D</sub>	DQ <sub>D</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQ <sub>A</sub>	DQ <sub>A</sub>
<b>N</b>	DQP <sub>D</sub>	NC	V <sub>DDQ</sub>	V <sub>SS</sub>	NC	NC	NC	V <sub>SS</sub>	V <sub>DDQ</sub>	NC	DQP <sub>A</sub>
<b>P</b>	NC/144M	NC/72M	A	A	TDI	A1	TDO	A	A	A	NC/288M
<b>R</b>	MODE	A	A	A	TMS	A0	TCK	A	A	A	A

**CY7C1463AV33 (2M x 18)**

	1	2	3	4	5	6	7	8	9	10	11
<b>A</b>	NC/576M	A	$\overline{CE}_1$	$\overline{BW}_B$	NC	$\overline{CE}_3$	$\overline{CEN}$	ADV/LD	A	A	A
<b>B</b>	NC/1G	A	CE2	NC	$\overline{BW}_A$	CLK	$\overline{WE}$	$\overline{OE}$	A	A	NC
<b>C</b>	NC	NC	V <sub>DDQ</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DDQ</sub>	NC	DQP <sub>A</sub>
<b>D</b>	NC	DQ <sub>B</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	NC	DQ <sub>A</sub>
<b>E</b>	NC	DQ <sub>B</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	NC	DQ <sub>A</sub>
<b>F</b>	NC	DQ <sub>B</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	NC	DQ <sub>A</sub>
<b>G</b>	NC	DQ <sub>B</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	NC	DQ <sub>A</sub>
<b>H</b>	NC	NC	NC	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	NC	NC	ZZ
<b>J</b>	DQ <sub>B</sub>	NC	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQ <sub>A</sub>	NC
<b>K</b>	DQ <sub>B</sub>	NC	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQ <sub>A</sub>	NC
<b>L</b>	DQ <sub>B</sub>	NC	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQ <sub>A</sub>	NC
<b>M</b>	DQ <sub>B</sub>	NC	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQ <sub>A</sub>	NC
<b>N</b>	DQP <sub>B</sub>	NC	V <sub>DDQ</sub>	V <sub>SS</sub>	NC	NC	NC	V <sub>SS</sub>	V <sub>DDQ</sub>	NC	NC
<b>P</b>	NC/144M	NC/72M	A	A	TDI	A1	TDO	A	A	A	NC/288M
<b>R</b>	MODE	A	A	A	TMS	A0	TCK	A	A	A	A

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**Pin Configurations** (continued)

**209-Ball FBGA (14 x 22 x 1.76 mm) Pinout**

**CY7C1465AV33 (512K × 72)**

	1	2	3	4	5	6	7	8	9	10	11
<b>A</b>	DQg	DQg	A	CE <sub>2</sub>	A	ADV/LD	A	CE <sub>3</sub>	A	DQb	DQb
<b>B</b>	DQg	DQg	BWS <sub>c</sub>	BWS <sub>g</sub>	NC	WE	A	BWS <sub>b</sub>	BWS <sub>f</sub>	DQb	DQb
<b>C</b>	DQg	DQg	BWS <sub>h</sub>	BWS <sub>d</sub>	NC/576M	CE <sub>1</sub>	NC	BWS <sub>e</sub>	BWS <sub>a</sub>	DQb	DQb
<b>D</b>	DQg	DQg	V <sub>SS</sub>	NC	NC/1G	OE	NC	NC	V <sub>SS</sub>	DQb	DQb
<b>E</b>	DQPg	DQPc	V <sub>DDQ</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>DD</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	V <sub>DDQ</sub>	DQPf	DQPb
<b>F</b>	DQc	DQc	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	NC	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	DQf	DQf
<b>G</b>	DQc	DQc	V <sub>DDQ</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	NC	V <sub>DD</sub>	V <sub>DDQ</sub>	V <sub>DDQ</sub>	DQf	DQf
<b>H</b>	DQc	DQc	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	NC	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	DQf	DQf
<b>J</b>	DQc	DQc	V <sub>DDQ</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	NC	V <sub>DD</sub>	V <sub>DDQ</sub>	V <sub>DDQ</sub>	DQf	DQf
<b>K</b>	NC	NC	CLK	NC	V <sub>SS</sub>	CEN	V <sub>SS</sub>	NC	NC	NC	NC
<b>L</b>	DQh	DQh	V <sub>DDQ</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	NC	V <sub>DD</sub>	V <sub>DDQ</sub>	V <sub>DDQ</sub>	DQa	DQa
<b>M</b>	DQh	DQh	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	NC	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	DQa	DQa
<b>N</b>	DQh	DQh	V <sub>DDQ</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	NC	V <sub>DD</sub>	V <sub>DDQ</sub>	V <sub>DDQ</sub>	DQa	DQa
<b>P</b>	DQh	DQh	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	ZZ	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	DQa	DQa
<b>R</b>	DQPd	DQPh	V <sub>DDQ</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>DD</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	V <sub>DDQ</sub>	DQPa	DQPe
<b>T</b>	DQd	DQd	V <sub>SS</sub>	NC	NC	MODE	NC	NC	V <sub>SS</sub>	DQe	DQe
<b>U</b>	DQd	DQd	NC/144M	A	NC/72M	A	A	A	NC/288M	DQe	DQe
<b>V</b>	DQd	DQd	A	A	A	A1	A	A	A	DQe	DQe
<b>W</b>	DQd	DQd	TMS	TDI	A	A0	A	TDO	TCK	DQe	DQe

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## Pin Definitions

Name	IO	Description
A <sub>0</sub> , A <sub>1</sub> , A	Input-Synchronous	<b>Address Inputs used to select one of the address locations.</b> Sampled at the rising edge of the CLK. A <sub>[1:0]</sub> are fed to the two-bit burst counter.
$\overline{BW}_A$ , $\overline{BW}_B$ $\overline{BW}_C$ , $\overline{BW}_D$ , $\overline{BW}_E$ , $\overline{BW}_F$ , $\overline{BW}_G$ , $\overline{BW}_H$	Input-Synchronous	<b>Byte Write Inputs, Active LOW.</b> Qualified with $\overline{WE}$ to conduct writes to the SRAM. Sampled on the rising edge of CLK.
$\overline{WE}$	Input-Synchronous	<b>Write Enable Input, Active LOW.</b> Sampled on the rising edge of CLK if $\overline{CEN}$ is active LOW. This signal must be asserted LOW to initiate a write sequence.
ADV/LD	Input-Synchronous	<b>Advance/Load Input.</b> Used to advance the on-chip address counter or load a new address. When HIGH (and CEN is asserted LOW) the internal burst counter is advanced. When LOW, a new address can be loaded into the device for an access. After being deselected, ADV/LD must be driven LOW to load a new address.
CLK	Input-Clock	<b>Clock Input.</b> Used to capture all synchronous inputs to the device. CLK is qualified with $\overline{CEN}$ . CLK is only recognized if CEN is active LOW.
$\overline{CE}_1$	Input-Synchronous	<b>Chip Enable 1 Input, Active LOW.</b> Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_2$ and $\overline{CE}_3$ to select/deselect the device.
$\overline{CE}_2$	Input-Synchronous	<b>Chip Enable 2 Input, Active HIGH.</b> Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and $\overline{CE}_3$ to select/deselect the device.
$\overline{CE}_3$	Input-Synchronous	<b>Chip Enable 3 Input, Active LOW.</b> Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and $\overline{CE}_2$ to select/deselect the device.
$\overline{OE}$	Input-Asynchronous	<b>Output Enable, asynchronous input, Active LOW.</b> Combined with the synchronous logic block inside the device to control the direction of the IO pins. When LOW, the IO pins are allowed to behave as outputs. When deasserted HIGH, IO pins are tri-stated, and act as input data pins. $\overline{OE}$ is masked during the data portion of a write sequence, during the first clock when emerging from a deselected state, when the device is deselected.
$\overline{CEN}$	Input-Synchronous	<b>Clock Enable Input, Active LOW.</b> When asserted LOW the Clock signal is recognized by the SRAM. When deasserted HIGH the Clock signal is masked. Since deasserting $\overline{CEN}$ does not deselect the device, use CEN to extend the previous cycle when required.
ZZ	Input-Asynchronous	<b>ZZ "Sleep" Input.</b> This active HIGH input places the device in a non-time critical "sleep" condition with data integrity preserved. During normal operation, this pin has to be LOW or left floating. ZZ pin has an internal pull down.
DQ <sub>s</sub>	IO-Synchronous	<b>Bidirectional Data IO lines.</b> As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by the addresses presented during the previous clock rise of the read cycle. The direction of the pins is controlled by $\overline{OE}$ . When $\overline{OE}$ is asserted LOW, the pins behave as outputs. When HIGH, DQ <sub>s</sub> and DQP <sub>[A:D]</sub> are placed in a tri-state condition. The outputs are automatically tri-stated during the data portion of a write sequence, during the first clock when emerging from a deselected state, and when the device is deselected, regardless of the state of $\overline{OE}$ .
DQP <sub>x</sub>	IO-Synchronous	<b>Bidirectional Data Parity IO Lines.</b> Functionally, these signals are identical to DQ <sub>s</sub> . During write sequences, DQP <sub>x</sub> is controlled by $\overline{BW}_x$ correspondingly.
MODE	Input Strap Pin	<b>Mode Input. Selects the burst order of the device.</b> When tied to Gnd selects linear burst sequence. When tied to V <sub>DD</sub> or left floating selects interleaved burst sequence.
V <sub>DD</sub>	Power Supply	<b>Power supply inputs to the core of the device.</b>
V <sub>DDQ</sub>	IO Power Supply	<b>Power supply for the IO circuitry.</b>
V <sub>SS</sub>	Ground	<b>Ground for the device.</b>



## Pin Definitions (continued)

Name	IO	Description
TDO	JTAG serial output Synchronous	<b>Serial data-out to the JTAG circuit.</b> Delivers data on the negative edge of TCK. If the JTAG feature is not used, leave this pin unconnected. This pin is not available on TQFP packages.
TDI	JTAG serial input Synchronous	<b>Serial data-In to the JTAG circuit.</b> Sampled on the rising edge of TCK. If the JTAG feature is not being used, this pin can be left floating or connected to V <sub>DD</sub> through a pull up resistor. This pin is not available on TQFP packages.
TMS	JTAG serial input Synchronous	<b>Serial data-In to the JTAG circuit.</b> Sampled on the rising edge of TCK. If the JTAG feature is not being used, this pin can be disconnected or connected to V <sub>DD</sub> . This pin is not available on TQFP packages.
TCK	JTAG-Clock	<b>Clock input to the JTAG circuitry.</b> If the JTAG feature is not being used, this pin must be connected to V <sub>SS</sub> . This pin is not available on TQFP packages.
NC	N/A	<b>No Connects.</b> Not internally connected to the die.
NC/72M	N/A	<b>Not connected to the die.</b> Can be tied to any voltage level.
NC/144M	N/A	<b>Not connected to the die.</b> Can be tied to any voltage level.
NC/288M	N/A	<b>Not connected to the die.</b> Can be tied to any voltage level.
NC/576M	N/A	<b>Not connected to the die.</b> Can be tied to any voltage level.
NC/1G	N/A	<b>Not connected to the die.</b> Can be tied to any voltage level.

## Functional Overview

The CY7C1461AV33/CY7C1463AV33/CY7C1465AV33 is a synchronous flow through burst SRAM designed specifically to eliminate wait states during Write-Read transitions. All synchronous inputs pass through input registers controlled by the rising edge of the clock. The clock signal is qualified with the Clock Enable input signal ( $\overline{CEN}$ ). If  $\overline{CEN}$  is HIGH, the clock signal is not recognized and all internal states are maintained. All synchronous operations are qualified with  $\overline{CEN}$ . Maximum access delay from the clock rise ( $t_{CDV}$ ) is 6.5 ns (133-MHz device).

Accesses can be initiated by asserting all three Chip Enables ( $\overline{CE}_1$ ,  $\overline{CE}_2$ ,  $\overline{CE}_3$ ) active at the rising edge of the clock. If Clock Enable ( $\overline{CEN}$ ) is active LOW and  $\overline{ADV/LD}$  is asserted LOW, the address presented to the device is latched. The access can either be a read or write operation, depending on the status of the Write Enable ( $\overline{WE}$ ).  $\overline{BW}_X$  can be used to conduct byte write operations.

Write operations are qualified by the Write Enable ( $\overline{WE}$ ). All writes are simplified with on-chip synchronous self timed write circuitry.

Three synchronous Chip Enables ( $\overline{CE}_1$ ,  $\overline{CE}_2$ ,  $\overline{CE}_3$ ) and an asynchronous Output Enable ( $\overline{OE}$ ) simplify depth expansion. All operations (Reads, Writes, and Deselects) are pipelined.  $\overline{ADV/LD}$  must be driven LOW after the device has been deselected to load a new address for the next operation.

### Single Read Accesses

A read access is initiated when these conditions are satisfied at clock rise:

- $\overline{CEN}$  is asserted LOW

- $\overline{CE}_1$ ,  $\overline{CE}_2$ , and  $\overline{CE}_3$  are ALL asserted active
- The Write Enable input signal  $\overline{WE}$  is deasserted HIGH
- $\overline{ADV/LD}$  is asserted LOW.

The address presented to the address inputs is latched into the Address Register and presented to the memory array and control logic. The control logic determines that a read access is in progress and allows the requested data to propagate to the output buffers. The data is available within 6.5 ns (133-MHz device) provided  $\overline{OE}$  is active LOW. After the first clock of the read access, the output buffers are controlled by  $\overline{OE}$  and the internal control logic.  $\overline{OE}$  must be driven LOW in order for the device to drive out the requested data. On the subsequent clock, another operation (Read/Write/Deselect) can be initiated. When the SRAM is deselected at clock rise by one of the chip enable signals, its output is tri-stated immediately.

### Burst Read Accesses

The CY7C1461AV33/CY7C1463AV33/CY7C1465AV33 has an on-chip burst counter that allows the user the ability to supply a single address and conduct up to four Reads without reasserting the address inputs.  $\overline{ADV/LD}$  must be driven LOW to load a new address into the SRAM, as described in the Single Read Access section above. The sequence of the burst counter is determined by the MODE input signal. A LOW input on MODE selects a linear burst mode, a HIGH selects an interleaved burst sequence. Both burst counters use A0 and A1 in the burst sequence, and wraps around when incremented sufficiently. A HIGH input on  $\overline{ADV/LD}$  increments the internal burst counter regardless of the state of chip enable inputs or  $\overline{WE}$ .  $\overline{WE}$  is latched at the beginning of a burst cycle. Therefore, the type of access (Read or Write) is maintained throughout the burst sequence.

### Single Write Accesses

Write access are initiated when the following conditions are satisfied at clock rise: (1)  $\overline{CEN}$  is asserted LOW, (2)  $\overline{CE}_1$ ,  $\overline{CE}_2$ , and  $\overline{CE}_3$  are ALL asserted active, and (3) the write signal  $\overline{WE}$  is asserted LOW. The address presented to the address bus is loaded into the Address Register. The write signals are latched into the Control Logic block. The data lines are automatically tri-stated regardless of the state of the OE input signal. This allows the external logic to present the data on DQs and DQP<sub>X</sub>.

On the next clock rise the data presented to DQs and DQP<sub>X</sub> (or a subset for byte write operations, see truth table for details) inputs is latched into the device and the write is complete. Additional accesses (Read/Write/Deselect) can be initiated on this cycle.

The data written during the Write operation is controlled by BW<sub>X</sub> signals. The CY7C1461AV33/CY7C1463AV33/CY7C1465AV33 provides byte write capability that is described in the truth table. Asserting the Write Enable input ( $\overline{WE}$ ) with the selected Byte Write Select input selectively writes to only the desired bytes. Bytes not selected during a byte write operation remains unaltered. A synchronous self timed write mechanism has been provided to simplify the write operations. Byte write capability has been included to greatly simplify Read/Modify/Write sequences, which can be reduced to simple byte write operations.

Because the CY7C1461AV33/CY7C1463AV33/CY7C1465AV33 is a common IO device, data must not be driven into the device while the outputs are active. The Output Enable (OE) can be deasserted HIGH before presenting data to the DQs and DQP<sub>X</sub> inputs. Doing so tri-states the output drivers. As a safety precaution, DQs and DQP<sub>X</sub> are automatically tri-stated during the data portion of a write cycle, regardless of the state of OE.

### Burst Write Accesses

The CY7C1461AV33/CY7C1463AV33/CY7C1465AV33 has an on-chip burst counter that allows the user the ability to supply a single address and conduct up to four Write operations without reasserting the address inputs. ADV/LD must be driven LOW to load the initial address, as described in the Single Write Access section above. When ADV/LD is driven

HIGH on the subsequent clock rise, the Chip Enables ( $\overline{CE}_1$ ,  $\overline{CE}_2$ , and  $\overline{CE}_3$ ) and WE inputs are ignored and the burst counter is incremented. The correct BW<sub>X</sub> inputs must be driven in each cycle of the burst write, to write the correct bytes of data.

### Interleaved Burst Address Table (MODE = Floating or V<sub>DD</sub>)

First Address A1: A0	Second Address A1: A0	Third Address A1: A0	Fourth Address A1: A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

### Linear Burst Address Table (MODE = GND)

First Address A1: A0	Second Address A1: A0	Third Address A1: A0	Fourth Address A1: A0
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

### Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation "sleep" mode. Two clock cycles are required to enter into or exit from this "sleep" mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the "sleep" mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected prior to entering the "sleep" mode.  $\overline{CE}_1$ ,  $\overline{CE}_2$ , and  $\overline{CE}_3$ , must remain inactive for the duration of  $t_{ZZREC}$  after the ZZ input returns LOW.

### ZZ Mode Electrical Characteristics

Parameter	Description	Test Conditions	Min	Max	Unit
I <sub>DDZZ</sub>	Sleep mode standby current	$ZZ \geq V_{DD} - 0.2V$		100	mA
t <sub>ZZS</sub>	Device operation to ZZ	$ZZ \geq V_{DD} - 0.2V$		2t <sub>CYC</sub>	ns
t <sub>ZZREC</sub>	ZZ recovery time	$ZZ \leq 0.2V$	2t <sub>CYC</sub>		ns
t <sub>ZZI</sub>	ZZ active to sleep current	This parameter is sampled		2t <sub>CYC</sub>	ns
t <sub>RZZI</sub>	ZZ Inactive to exit sleep current	This parameter is sampled	0		ns

**Truth Table**<sup>[2, 3, 4, 5, 6, 7, 8]</sup>

Operation	Address Used	$\overline{CE}_1$	$CE_2$	$\overline{CE}_3$	ZZ	ADV/LD	$\overline{WE}$	$\overline{BW}_x$	$\overline{OE}$	$\overline{CEN}$	CLK	DQ
Deselect Cycle	None	H	X	X	L	L	X	X	X	L	L->H	Tri-State
Deselect Cycle	None	X	X	H	L	L	X	X	X	L	L->H	Tri-State
Deselect Cycle	None	X	L	X	L	L	X	X	X	L	L->H	Tri-State
Continue Deselect Cycle	None	X	X	X	L	H	X	X	X	L	L->H	Tri-State
Read Cycle (Begin Burst)	External	L	H	L	L	L	H	X	L	L	L->H	Data Out (Q)
Read Cycle (Continue Burst)	Next	X	X	X	L	H	X	X	L	L	L->H	Data Out (Q)
NOP/Dummy Read (Begin Burst)	External	L	H	L	L	L	H	X	H	L	L->H	Tri-State
Dummy Read (Continue Burst)	Next	X	X	X	L	H	X	X	H	L	L->H	Tri-State
Write Cycle (Begin Burst)	External	L	H	L	L	L	L	L	X	L	L->H	Data In (D)
Write Cycle (Continue Burst)	Next	X	X	X	L	H	X	L	X	L	L->H	Data In (D)
NOP/Write Abort (Begin Burst)	None	L	H	L	L	L	L	H	X	L	L->H	Tri-State
Write Abort (Continue Burst)	Next	X	X	X	L	H	X	H	X	L	L->H	Tri-State
Ignore Clock Edge (Stall)	Current	X	X	X	L	X	X	X	X	H	L->H	-
Sleep Mode	None	X	X	X	H	X	X	X	X	X	X	Tri-State

**Notes:**

- X = "Don't Care." H = Logic HIGH, L = Logic LOW.  $\overline{BW}_x = L$  signifies at least one Byte Write Select is active,  $\overline{BW}_x = Valid$  signifies that the desired byte write selects are asserted, see truth table for details.
- Write is defined by  $\overline{BW}_x$ , and  $\overline{WE}$ . See truth table for Read/Write.
- When a write cycle is detected, all IOs are tri-stated, even during byte writes.
- The DQs and  $DQP_x$  pins are controlled by the current cycle and the  $\overline{OE}$  signal.  $\overline{OE}$  is asynchronous and is not sampled with the clock.
- $CEN = H$ , inserts wait states.
- Device powers up deselected and the IOs in a tri-state condition, regardless of  $\overline{OE}$ .
- $\overline{OE}$  is asynchronous and is not sampled with the clock rise. It is masked internally during write cycles. During a read cycle DQs and  $DQP_x = Tri-state$  when  $\overline{OE}$  is inactive or when the device is deselected, and DQs and  $DQP_x = data$  when  $\overline{OE}$  is active.

**Truth Table for Read/Write<sup>[2, 9]</sup>**

Function (CY7C1461AV33)	$\overline{WE}$	$\overline{BW}_A$	$\overline{BW}_B$	$\overline{BW}_C$	$\overline{BW}_D$
Read	H	X	X	X	X
Write No bytes written	L	H	H	H	H
Write Byte A – (DQ <sub>A</sub> and DQP <sub>A</sub> )	L	L	H	H	H
Write Byte B – (DQ <sub>B</sub> and DQP <sub>B</sub> )	L	H	L	H	H
Write Byte C – (DQ <sub>C</sub> and DQP <sub>C</sub> )	L	H	H	L	H
Write Byte D – (DQ <sub>D</sub> and DQP <sub>D</sub> )	L	H	H	H	L
Write All Bytes	L	L	L	L	L

**Truth Table for Read/Write<sup>[2, 9]</sup>**

Function (CY7C1463AV33)	$\overline{WE}$	$\overline{BW}_b$	$\overline{BW}_a$
Read	H	X	X
Write – No Bytes Written	L	H	H
Write Byte a – (DQ <sub>a</sub> and DQP <sub>a</sub> )	L	H	L
Write Byte b – (DQ <sub>b</sub> and DQP <sub>b</sub> )	L	L	H
Write Both Bytes	L	L	L

**Truth Table for Read/Write<sup>[2, 9]</sup>**

Function (CY7C1465AV33)	$\overline{WE}$	$\overline{BW}_x$
Read	H	X
Write – No Bytes Written	L	H
Write Byte X – (DQ <sub>x</sub> and DQP <sub>x</sub> )	L	L
Write All Bytes	L	All $\overline{BW} = L$

**Note:**

9. Table only lists a partial listing of the byte write combinations. Any Combination of  $\overline{BW}_x$  is valid Appropriate write is done based on which byte write is active

## IEEE 1149.1 Serial Boundary Scan (JTAG)

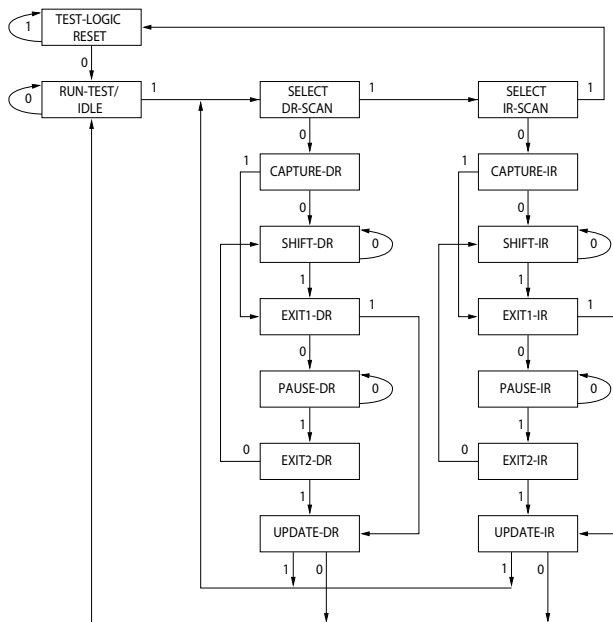
The CY7C1461AV33/CY7C1463AV33/CY7C1465AV33 incorporates a serial boundary scan test access port (TAP). This part is fully compliant with 1149.1. The TAP operates using JEDEC-standard 3.3V/2.5V IO logic level.

The CY7C1461AV33/CY7C1463AV33/CY7C1465AV33 contains a TAP controller, instruction register, boundary scan register, bypass register, and ID register.

### Disabling the JTAG Feature

It is possible to operate the SRAM without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW ( $V_{SS}$ ) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. They may alternately be connected to  $V_{DD}$  through a pull up resistor. TDO must be left unconnected. Upon power up, the device is up in a reset state which does not interfere with the operation of the device.

### TAP Controller State Diagram



The 0/1 next to each state represents the value of TMS at the rising edge of TCK.

### Test Access Port (TAP)

#### Test Clock (TCK)

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

#### Test Mode Select (TMS)

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. It is allowable to leave this ball unconnected if the TAP is not used. The ball is pulled up internally, resulting in a logic HIGH level.

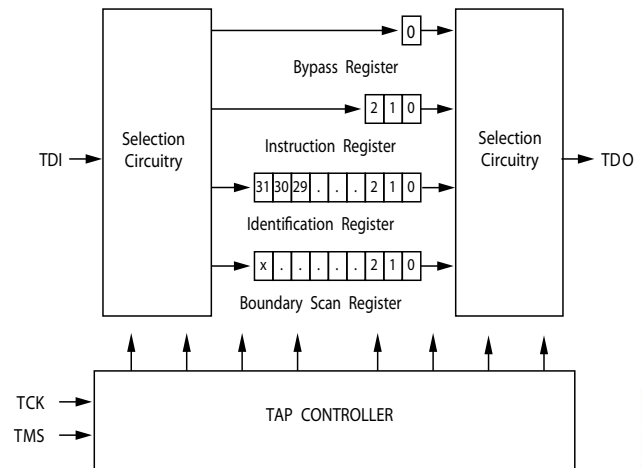
### Test Data In (TDI)

The TDI ball is used to serially input information into the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSB) of any register. (See Tap Controller Block Diagram.)

### Test Data Out (TDO)

The TDO output ball is used to serially clock data-out from the registers. The output is active depending upon the current state of the TAP state machine. The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register. (See Tap Controller State Diagram.)

### TAP Controller Block Diagram



### Performing a TAP Reset

A RESET is performed by forcing TMS HIGH ( $V_{DD}$ ) for five rising edges of TCK. This RESET does not affect the operation of the SRAM and may be performed while the SRAM is operating.

At power up, the TAP is reset internally to ensure that TDO comes up in a High-Z state.

### TAP Registers

Registers are connected between the TDI and TDO balls and allow data to be scanned into and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction register. Data is serially loaded into the TDI ball on the rising edge of TCK. Data is output on the TDO ball on the falling edge of TCK.

#### Instruction Register

Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO balls as shown in the Tap Controller Block Diagram. Upon power up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section.

When the TAP controller is in the Capture-IR state, the two least significant bits are loaded with a binary “01” pattern to allow for fault isolation of the board-level serial test data path.

#### *Bypass Register*

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single-bit register that can be placed between the TDI and TDO balls. This allows data to be shifted through the SRAM with minimal delay. The bypass register is set LOW ( $V_{SS}$ ) when the BYPASS instruction is executed.

#### *Boundary Scan Register*

The boundary scan register is connected to all the input and bidirectional balls on the SRAM. The length of the Boundary Scan Register for the SRAM in different packages is listed in the Scan Register Sizes table.

The boundary scan register is loaded with the contents of the RAM IO ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO balls when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD and SAMPLE Z instructions can be used to capture the contents of the IO ring.

The Boundary Scan Order tables show the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

#### *Identification (ID) Register*

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in the Identification Register Definitions table.

### **TAP Instruction Set**

#### *Overview*

Eight different instructions are possible with the three bit instruction register. All combinations are listed in the Instruction Codes table. Three of these instructions are listed as RESERVED and must not be used. The other five instructions are described in detail below.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO balls. To execute the instruction after it is shifted in, the TAP controller needs to be moved into the Update-IR state.

#### *IDCODE*

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO balls and allows the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state.

The IDCODE instruction is loaded into the instruction register upon power up or whenever the TAP controller is supplied a test logic reset state.

#### *SAMPLE Z*

The SAMPLE Z instruction causes the boundary scan register to be connected between the TDI and TDO pins when the TAP controller is in a Shift-DR state. The SAMPLE Z command puts the output bus into a High-Z state until the next command is supplied during the “Update IR” state.

#### *SAMPLE/PRELOAD*

SAMPLE/PRELOAD is a 1149.1 mandatory instruction. When the SAMPLE/PRELOAD instructions are loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the inputs and output pins is captured in the boundary scan register.

The user must be aware that the TAP controller clock can only operate at a frequency up to 20 MHz, while the SRAM clock operates more than an order of magnitude faster. Because there is a large difference in the clock frequencies, it is possible that during the Capture-DR state, an input or output undergoes a transition. The TAP may then try to capture a signal while in transition (metastable state). This does not harm the device, but there is no guarantee as to the value that is captured. Repeatable results may not be possible.

To guarantee that the boundary scan register captures the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller's capture setup plus hold times ( $t_{CS}$  and  $t_{CH}$ ). The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CK and  $\overline{CK}$  captured in the boundary scan register.

Once the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO pins.

PRELOAD allows an initial data pattern to be placed at the latched parallel outputs of the boundary scan register cells prior to the selection of another boundary scan test operation.

The shifting of data for the SAMPLE and PRELOAD phases can occur concurrently when required—that is, while data captured is shifted out, the preloaded data can be shifted in.

#### *BYPASS*

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between the TDI and TDO pins. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

#### *EXTEST*

The EXTEST instruction enables the preloaded data to be driven out through the system output pins. This instruction also selects the boundary scan register to be connected for serial access between the TDI and TDO in the shift-DR controller state.

### EXTEST OUTPUT BUS TRI-STATE

IEEE Standard 1149.1 mandates that the TAP controller be able to put the output bus into a tri-state mode.

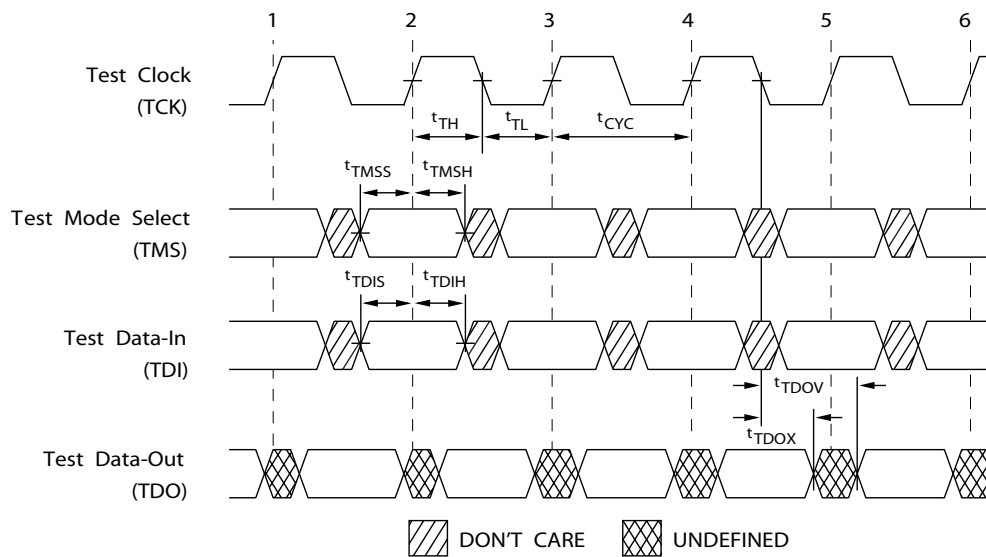
The boundary scan register has a special bit located at bit #89 (for 165-FBGA package) or bit #138 (for 209 FBGA package). When this scan cell, called the “extest output bus tri-state”, is latched into the preload register during the “Update-DR” state in the TAP controller, it directly controls the state of the output (Q-bus) pins, when the EXTEST is entered as the current instruction. When HIGH, it enables the output buffers to drive the output bus. When LOW, this bit places the output bus into a High-Z condition.

This bit can be set by entering the SAMPLE/PRELOAD or EXTEST command, and then shifting the desired bit into that cell, during the “Shift-DR” state. During “Update-DR”, the value loaded into that shift-register cell latches into the preload register. When the EXTEST instruction is entered, this bit directly controls the output Q-bus pins. Note that this bit is pre-set HIGH to enable the output when the device is powered-up, and also when the TAP controller is in the “Test-Logic-Reset” state.

### Reserved

These instructions are not implemented but are reserved for future use. Do not use these instructions.

### TAP Timing



NOT RECOMMENDED FOR NEW DESIGNS  
 ONE OR MORE ORDERABLE PARTS ASSOCIATED WITH THIS DOCUMENT IS OBSOLETE. FOR  
 REPLACEMENT PART INQUIRIES, PLEASE CONTACT YOUR LOCAL SALES REPRESENTATIVE

## TAP AC Switching Characteristics

Over the Operating Range<sup>[10, 11]</sup>

Parameter	Description	Min	Max	Unit
<b>Clock</b>				
$t_{TCYC}$	TCK Clock Cycle Time	50		ns
$t_{TF}$	TCK Clock Frequency		20	MHz
$t_{TH}$	TCK Clock HIGH time	20		ns
$t_{TL}$	TCK Clock LOW time	20		ns
<b>Output Times</b>				
$t_{TDOV}$	TCK Clock LOW to TDO Valid		10	ns
$t_{TDOX}$	TCK Clock LOW to TDO Invalid	0		ns
<b>Setup Times</b>				
$t_{TMSS}$	TMS Setup to TCK Clock Rise	5		ns
$t_{TDIS}$	TDI Setup to TCK Clock Rise	5		ns
$t_{CS}$	Capture Setup to TCK Rise	5		ns
<b>Hold Times</b>				
$t_{TMSH}$	TMS Hold after TCK Clock Rise	5		ns
$t_{TDIH}$	TDI Hold after Clock Rise	5		ns
$t_{CH}$	Capture Hold after Clock Rise	5		ns

**Notes:**

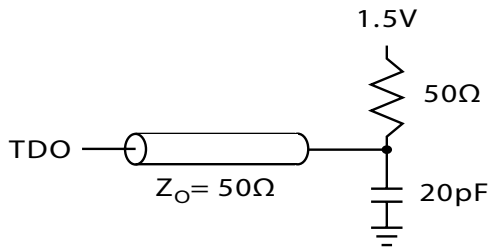
- 10.  $t_{CS}$  and  $t_{CH}$  refer to the setup and hold time requirements of latching data from the boundary scan register.
- 11. Test conditions are specified using the load in TAP AC test Conditions.  $t_r/t_f = 1$  ns.



### 3.3V TAP AC Test Conditions

Input pulse levels .....  $V_{SS}$  to 3.3V  
 Input rise and fall times ..... 1 ns  
 Input timing reference levels ..... 1.5V  
 Output reference levels ..... 1.5V  
 Test load termination supply voltage ..... 1.5V

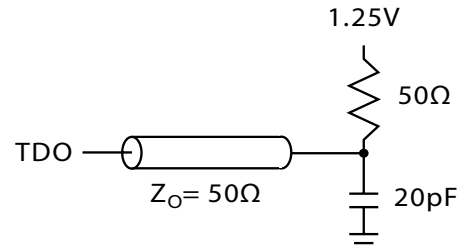
### 3.3V TAP AC Output Load Equivalent



### 2.5V TAP AC Test Conditions

Input pulse levels .....  $V_{SS}$  to 2.5V  
 Input rise and fall time ..... 1 ns  
 Input timing reference levels ..... 1.25V  
 Output reference levels ..... 1.25V  
 Test load termination supply voltage ..... 1.25V

### 2.5V TAP AC Output Load Equivalent



### TAP DC Electrical Characteristics And Operating Conditions

( $0^{\circ}\text{C} < T_A < +70^{\circ}\text{C}$ ;  $V_{DD} = 3.135$  to  $3.6\text{V}$  unless otherwise noted)<sup>[12]</sup>

Parameter	Description	Test Conditions	Min	Max	Unit	
$V_{OH1}$	Output HIGH Voltage	$I_{OH} = -4.0\text{ mA}$ , $V_{DDQ} = 3.3\text{V}$	2.4		V	
		$I_{OH} = -1.0\text{ mA}$ , $V_{DDQ} = 2.5\text{V}$	2.0		V	
$V_{OH2}$	Output HIGH Voltage	$I_{OH} = -100\text{ }\mu\text{A}$	$V_{DDQ} = 3.3\text{V}$	2.9		V
			$V_{DDQ} = 2.5\text{V}$	2.1		V
$V_{OL1}$	Output LOW Voltage	$I_{OL} = 8.0\text{ mA}$	$V_{DDQ} = 3.3\text{V}$		0.4	V
		$I_{OL} = 1.0\text{ mA}$	$V_{DDQ} = 2.5\text{V}$		0.4	V
$V_{OL2}$	Output LOW Voltage	$I_{OL} = 100\text{ }\mu\text{A}$	$V_{DDQ} = 3.3\text{V}$		0.2	V
			$V_{DDQ} = 2.5\text{V}$		0.2	V
$V_{IH}$	Input HIGH Voltage		$V_{DDQ} = 3.3\text{V}$	2.0	$V_{DD} + 0.3$	V
			$V_{DDQ} = 2.5\text{V}$	1.7	$V_{DD} + 0.3$	V
$V_{IL}$	Input LOW Voltage		$V_{DDQ} = 3.3\text{V}$	-0.3	0.8	V
			$V_{DDQ} = 2.5\text{V}$	-0.3	0.7	V
$I_X$	Input Load Current	$GND \leq V_{IN} \leq V_{DDQ}$	-5	5	$\mu\text{A}$	

**Note:**

12. All voltages referenced to  $V_{SS}$  (GND).

### Identification Register Definitions

Instruction Field	CY7C1461AV33 (1M x 36)	CY7C1463AV33 (2M x 18)	CY7C1465AV33 (512K x 72)	Description
Revision Number (31:29)	000	000	000	Describes the version number
Device Depth (28:24) <sup>[13]</sup>	01011	01011	01011	Reserved for internal use
Architecture/Memory Type (23:18)	001001	001001	001001	Defines memory type and architecture
Bus Width/Density(17:12)	100111	010111	110111	Defines width and density
Cypress JEDEC ID Code (11:1)	00000110100	00000110100	00000110100	Allows unique identification of SRAM vendor
ID Register Presence Indicator (0)	1	1	1	Indicates the presence of an ID register

### Scan Register Sizes

Register Name	Bit Size (x36)	Bit Size (x18)	Bit Size (x72)
Instruction	3	3	3
Bypass	1	1	1
ID	32	32	32
Boundary Scan Order (165-Ball FBGA package)	89	89	–
Boundary Scan Order (209-Ball FBGA package)	–	–	138

### Identification Codes

Instruction	Code	Description
EXTEST	000	Captures IO ring contents. Places the boundary scan register between TDI and TDO. Forces all SRAM outputs to High-Z state.
IDCODE	001	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operations.
SAMPLE Z	010	Captures IO ring contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a High-Z state.
RESERVED	011	Do Not Use: This instruction is reserved for future use.
SAMPLE/PRELOAD	100	Captures IO ring contents. Places the boundary scan register between TDI and TDO. Does not affect SRAM operation.
RESERVED	101	Do Not Use: This instruction is reserved for future use.
RESERVED	110	Do Not Use: This instruction is reserved for future use.
BYPASS	111	Places the bypass register between TDI and TDO. This operation does not affect SRAM operations.

**Note:**

13. Bit #24 is “1” in the ID Register Definitions for both 2.5V and 3.3V versions of this device.



**209-Ball FBGA Boundary Scan Order** <sup>[15]</sup>

**CY7C1465AV33 (512K x 72)**

Bit#	Ball ID
1	W6
2	V6
3	U6
4	W7
5	V7
6	U7
7	T7
8	V8
9	U8
10	T8
11	V9
12	U9
13	P6
14	W11
15	W10
16	V11
17	V10
18	U11
19	U10
20	T11
21	T10
22	R11
23	R10
24	P11
25	P10
26	N11
27	N10
28	M11
29	M10
30	L11
31	L10
32	K11
33	M6
34	L6
35	J6

Bit#	Ball ID
36	F6
37	K8
38	K9
39	K10
40	J11
41	J10
42	H11
43	H10
44	G11
45	G10
46	F11
47	F10
48	E10
49	E11
50	D11
51	D10
52	C11
53	C10
54	B11
55	B10
56	A11
57	A10
58	C9
59	B9
60	A9
61	D8
62	C8
63	B8
64	A8
65	D7
66	C7
67	B7
68	A7
69	D6
70	G6

Bit#	Ball ID
71	H6
72	C6
73	B6
74	A6
75	A5
76	B5
77	C5
78	D5
79	D4
80	C4
81	A4
82	B4
83	C3
84	B3
85	A3
86	A2
87	A1
88	B2
89	B1
90	C2
91	C1
92	D2
93	D1
94	E1
95	E2
96	F2
97	F1
98	G1
99	G2
100	H2
101	H1
102	J2
103	J1
104	K1
105	N6

Bit#	Ball ID
106	K3
107	K4
108	K6
109	K2
110	L2
111	L1
112	M2
113	M1
114	N2
115	N1
116	P2
117	P1
118	R2
119	R1
120	T2
121	T1
122	U2
123	U1
124	V2
125	V1
126	W2
127	W1
128	T6
129	U3
130	V3
131	T4
132	T5
133	U4
134	V4
135	W5
136	V5
137	U5
138	Internal

**Note:**  
 15. Bit# 138 is preset HIGH.

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## Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature .....	-65°C to +150°C
Ambient Temperature with Power Applied .....	-55°C to +125°C
Supply Voltage on V <sub>DD</sub> Relative to GND.....	-0.5V to +4.6V
Supply Voltage on V <sub>DDQ</sub> Relative to GND .....	-0.5V to +V <sub>DD</sub>
DC Voltage Applied to Outputs in Tri-State.....	-0.5V to V <sub>DDQ</sub> + 0.5V

DC Input Voltage .....	-0.5V to V <sub>DD</sub> + 0.5V
Current into Outputs (LOW).....	20 mA
Static Discharge Voltage.....	>2001V (MIL-STD-883, Method 3015)
Latch-up Current.....	>200 mA

## Operating Range

Range	Ambient Temperature	V <sub>DD</sub>	V <sub>DDQ</sub>
Commercial	0°C to +70°C	3.3V -5%/+10%	2.5V - 5% to V <sub>DD</sub>
Industrial	-40°C to +85°C		

## Electrical Characteristics

Over the Operating Range<sup>[16, 17]</sup>

Parameter	Description	Test Conditions	Min	Max	Unit
V <sub>DD</sub>	Power Supply Voltage		3.135	3.6	V
V <sub>DDQ</sub>	IO Supply Voltage	for 3.3V IO	3.135	V <sub>DD</sub>	V
		for 2.5V IO	2.375	2.625	V
V <sub>OH</sub>	Output HIGH Voltage	for 3.3V IO, I <sub>OH</sub> = -4.0 mA	2.4		V
		for 2.5V IO, I <sub>OH</sub> = -1.0 mA	2.0		V
V <sub>OL</sub>	Output LOW Voltage	for 3.3V IO, I <sub>OL</sub> = 8.0 mA		0.4	V
		for 2.5V IO, I <sub>OL</sub> = 1.0 mA		0.4	V
V <sub>IH</sub>	Input HIGH Voltage <sup>[16]</sup>	for 3.3V IO	2.0	V <sub>DD</sub> + 0.3V	V
		for 2.5V IO	1.7	V <sub>DD</sub> + 0.3V	V
V <sub>IL</sub>	Input LOW Voltage <sup>[16]</sup>	for 3.3V IO	-0.3	0.8	V
		for 2.5V IO	-0.3	0.7	V
I <sub>X</sub>	Input Leakage Current except ZZ and MODE	GND ≤ V <sub>I</sub> ≤ V <sub>DDQ</sub>	-5	5	μA
	Input Current of MODE	Input = V <sub>SS</sub>	-30		μA
		Input = V <sub>DD</sub>		5	μA
	Input Current of ZZ	Input = V <sub>SS</sub>	-5		μA
Input = V <sub>DD</sub>			30	μA	
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>DDQ</sub> , Output Disabled	-5	5	μA
I <sub>DD</sub>	V <sub>DD</sub> Operating Supply Current	V <sub>DD</sub> = Max., I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub> = 1/t <sub>CYC</sub>	7.5 ns cycle, 133 MHz	310	mA
			10 ns cycle, 100 MHz	290	mA
I <sub>SB1</sub>	Automatic CE Power down Current—TTL Inputs	V <sub>DD</sub> = Max, Device Deselected, V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub> , inputs switching	7.5 ns cycle, 133 MHz	180	mA
			10 ns cycle, 100 MHz	180	mA
I <sub>SB2</sub>	Automatic CE Power down Current—CMOS Inputs	V <sub>DD</sub> = Max, Device Deselected, V <sub>IN</sub> ≤ 0.3V or V <sub>IN</sub> ≥ V <sub>DD</sub> - 0.3V, f = 0, inputs static	All speeds	120	mA
I <sub>SB3</sub>	Automatic CE Power down Current—CMOS Inputs	V <sub>DD</sub> = Max, Device Deselected, or V <sub>IN</sub> ≤ 0.3V or V <sub>IN</sub> ≥ V <sub>DDQ</sub> - 0.3V, f = f <sub>MAX</sub> , inputs switching	7.5 ns cycle, 133 MHz	180	mA
			10 ns cycle, 100 MHz	180	mA
I <sub>SB4</sub>	Automatic CE Power down Current—TTL Inputs	V <sub>DD</sub> = Max, Device Deselected, V <sub>IN</sub> ≥ V <sub>DD</sub> - 0.3V or V <sub>IN</sub> ≤ 0.3V, f = 0, inputs static	All Speeds	135	mA

### Notes:

16. Overshoot: V<sub>IH</sub>(AC) < V<sub>DD</sub> + 1.5V (Pulse width less than t<sub>CYC</sub>/2), undershoot: V<sub>IL</sub>(AC) > -2V (Pulse width less than t<sub>CYC</sub>/2).  
 17. T<sub>Power-up</sub>: Assumes a linear ramp from 0V to V<sub>DD</sub>(min.) within 200 ms. During this time V<sub>IH</sub> < V<sub>DD</sub> and V<sub>DDQ</sub> ≤ V<sub>DD</sub>.

### Capacitance<sup>[18]</sup>

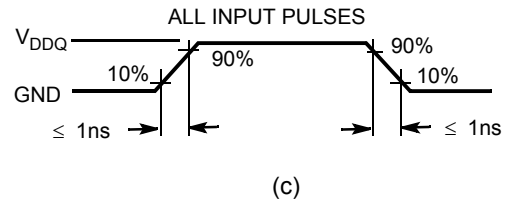
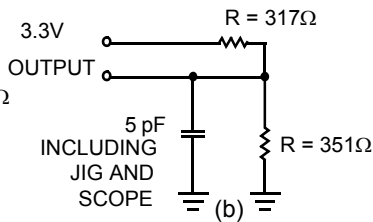
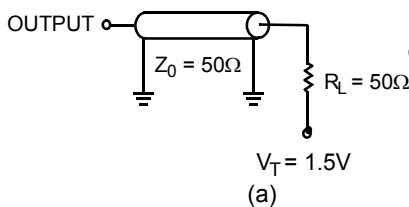
Parameter	Description	Test Conditions	100 TQFP Max	165 FBGA Max	209 FBGA Max	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>DD</sub> = 3.3V V <sub>DDQ</sub> = 2.5V	6.5	7	5	pF
C <sub>CLK</sub>	Clock Input Capacitance		3	7	5	pF
C <sub>IO</sub>	Input/Output Capacitance		5.5	6	7	pF

### Thermal Resistance<sup>[18]</sup>

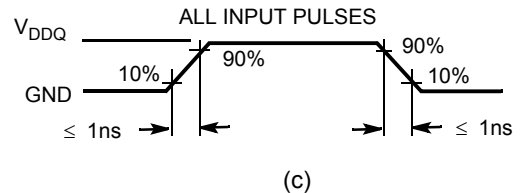
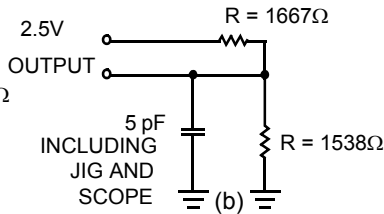
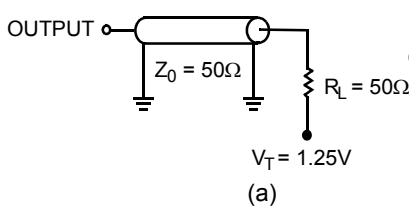
Parameter	Description	Test Conditions	100 TQFP Package	165 FBGA Package	209 FBGA Package	Unit
Θ <sub>JA</sub>	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, according to EIA/JESD51.	25.21	20.8	25.31	°C/W
Θ <sub>JC</sub>	Thermal Resistance (Junction to Case)		2.28	3.2	4.48	°C/W

### AC Test Loads and Waveforms

#### 3.3V IO Test Load



#### 2.5V IO Test Load



**Note:**

18. Tested initially and after any design or process change that may affect these parameters.

## Switching Characteristics

Over the Operating Range<sup>[23, 24]</sup>

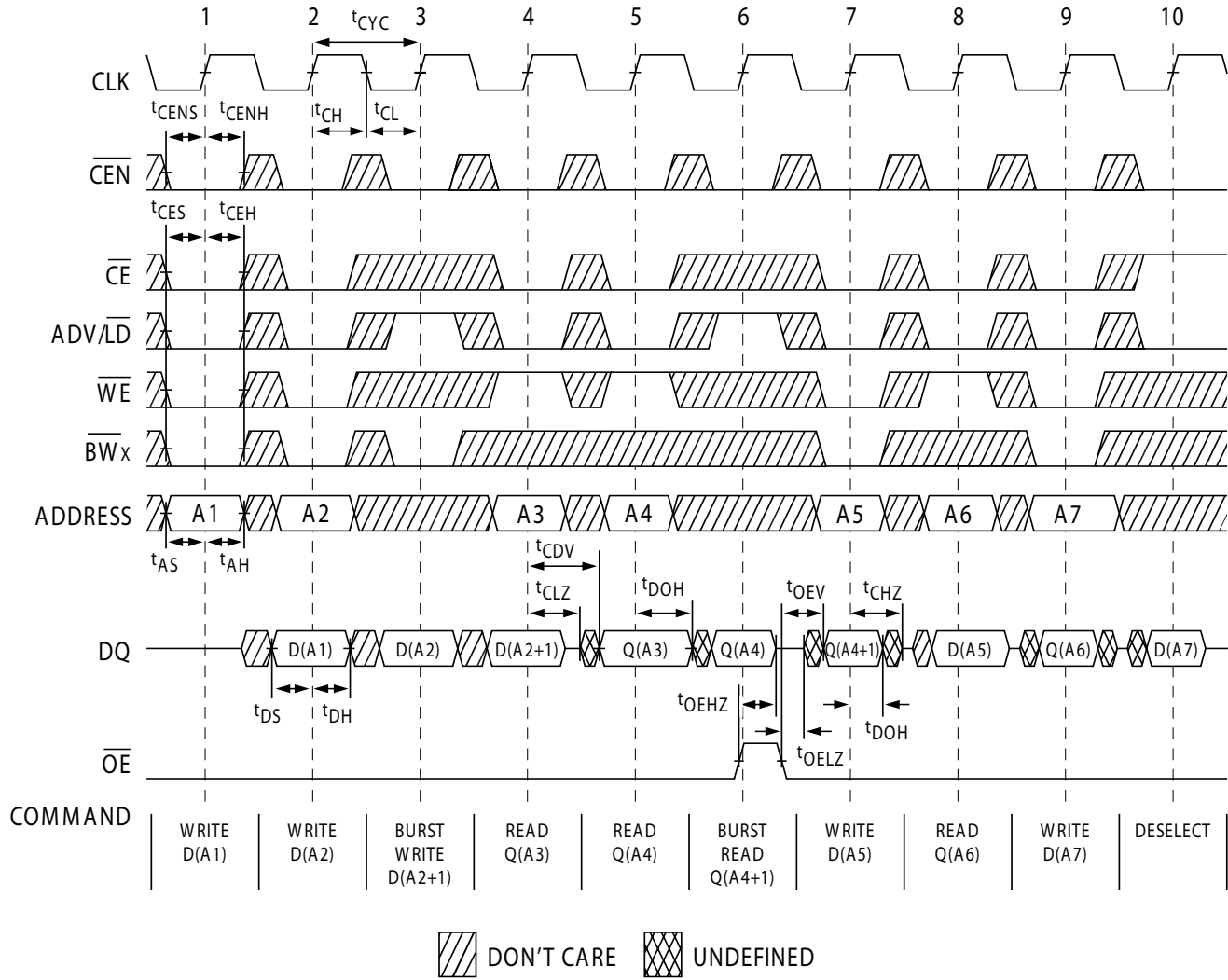
Parameter	Description	133 MHz		100 MHz		Unit
		Min	Max	Min	Max	
$t_{POWER}^{[19]}$		1		1		ms
<b>Clock</b>						
$t_{CYC}$	Clock Cycle Time	7.5		10		ns
$t_{CH}$	Clock HIGH	2.5		3.0		ns
$t_{CL}$	Clock LOW	2.5		3.0		ns
<b>Output Times</b>						
$t_{CDV}$	Data Output Valid After CLK Rise		6.5		8.5	ns
$t_{DOH}$	Data Output Hold After CLK Rise	2.5		2.5		ns
$t_{CLZ}$	Clock to Low-Z <sup>[20, 21, 22]</sup>	2.5		2.5		ns
$t_{CHZ}$	Clock to High-Z <sup>[20, 21, 22]</sup>		3.8	0	4.5	ns
$t_{OE\bar{V}}$	$\overline{OE}$ LOW to Output Valid		3.0		3.8	ns
$t_{OE\bar{L}Z}$	$\overline{OE}$ LOW to Output Low-Z <sup>[20, 21, 22]</sup>	0		0		ns
$t_{OE\bar{H}Z}$	$\overline{OE}$ HIGH to Output High-Z <sup>[20, 21, 22]</sup>		3.0		4.0	ns
<b>Setup Times</b>						
$t_{AS}$	Address Setup Before CLK Rise	1.5		1.5		ns
$t_{ALS}$	$\overline{ADV}/\overline{LD}$ Setup Before CLK Rise	1.5		1.5		ns
$t_{WES}$	$\overline{WE}$ , $\overline{BW}_x$ Setup Before CLK Rise	1.5		1.5		ns
$t_{CENS}$	$\overline{CEN}$ Setup Before CLK Rise	1.5		1.5		ns
$t_{DS}$	Data Input Setup Before CLK Rise	1.5		1.5		ns
$t_{CES}$	Chip Enable Setup Before CLK Rise	1.5		1.5		ns
<b>Hold Times</b>						
$t_{AH}$	Address Hold After CLK Rise	0.5		0.5		ns
$t_{ALH}$	$\overline{ADV}/\overline{LD}$ Hold After CLK Rise	0.5		0.5		ns
$t_{WEH}$	$\overline{WE}$ , $\overline{BW}_x$ Hold After CLK Rise	0.5		0.5		ns
$t_{CENH}$	$\overline{CEN}$ Hold After CLK Rise	0.5		0.5		ns
$t_{DH}$	Data Input Hold After CLK Rise	0.5		0.5		ns
$t_{CEH}$	Chip Enable Hold After CLK Rise	0.5		0.5		ns

### Notes:

19. This part has a voltage regulator internally;  $t_{POWER}$  is the time that the power needs to be supplied above  $V_{DD}$ (minimum) initially, before a read or write operation can be initiated.
20.  $t_{CHZ}$ ,  $t_{CLZ}$ ,  $t_{OE\bar{L}Z}$ , and  $t_{OE\bar{H}Z}$  are specified with AC test conditions shown in part (b) of AC Test Loads. Transition is measured  $\pm 200$  mV from steady-state voltage.
21. At any voltage and temperature,  $t_{OE\bar{H}Z}$  is less than  $t_{OE\bar{L}Z}$  and  $t_{CHZ}$  is less than  $t_{CLZ}$  to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve High-Z prior to Low-Z under the same system conditions.
22. This parameter is sampled and not 100% tested.
23. Timing reference level is 1.5V when  $V_{DDQ} = 3.3V$  and is 1.25V when  $V_{DDQ} = 2.5V$ .
24. Test conditions shown in (a) of AC Test Loads unless otherwise noted.

## Switching Waveforms

### Read/Write Waveforms<sup>[25, 26, 27]</sup>



**Notes:**

25. For this waveform ZZ is tied LOW.

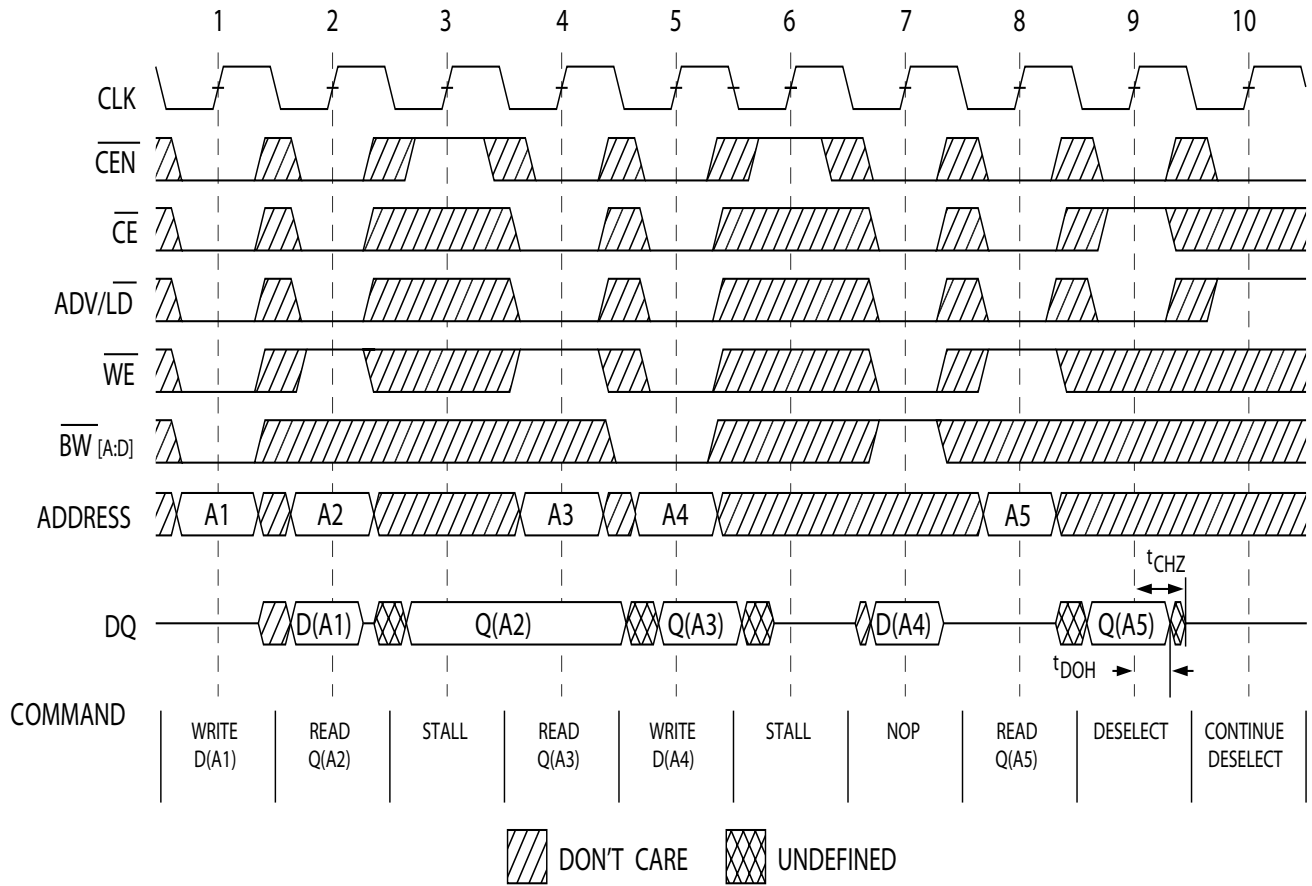
26. When  $\overline{CE}$  is LOW,  $\overline{CE}_1$  is LOW,  $CE_2$  is HIGH and  $\overline{CE}_3$  is LOW. When  $\overline{CE}$  is HIGH,  $\overline{CE}_1$  is HIGH or  $CE_2$  is LOW or  $\overline{CE}_3$  is HIGH.

27. Order of the Burst sequence is determined by the status of the MODE (0 = Linear, 1 = Interleaved). Burst operations are optional.



**Switching Waveforms (continued)**

**NOP, STALL and DESELECT Cycles**<sup>[25, 26, 28]</sup>



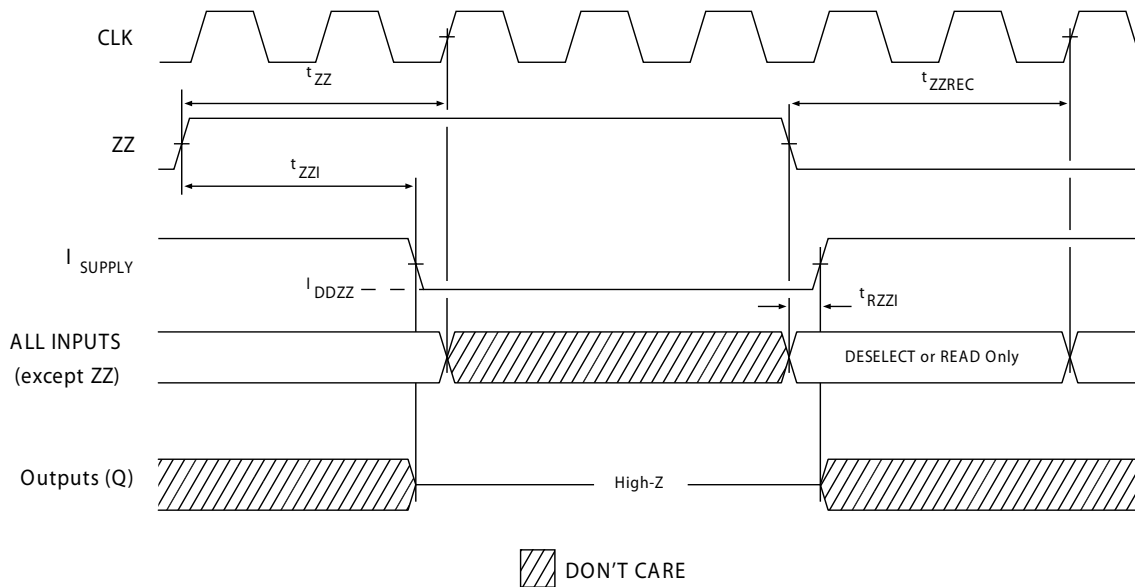
**Note:**

28. The IGNORE CLOCK EDGE or STALL cycle (Clock 3) illustrates  $\overline{CEN}$  being used to create a pause. A write is not performed during this cycle.

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Switching Waveforms (continued)

ZZ Mode Timing<sup>[29, 30]</sup>



Notes:

- 29. Device must be deselected when entering ZZ mode. See truth table for all possible signal conditions to deselect the device.
- 30. DQs are in High-Z when exiting ZZ sleep mode.

### Ordering Information

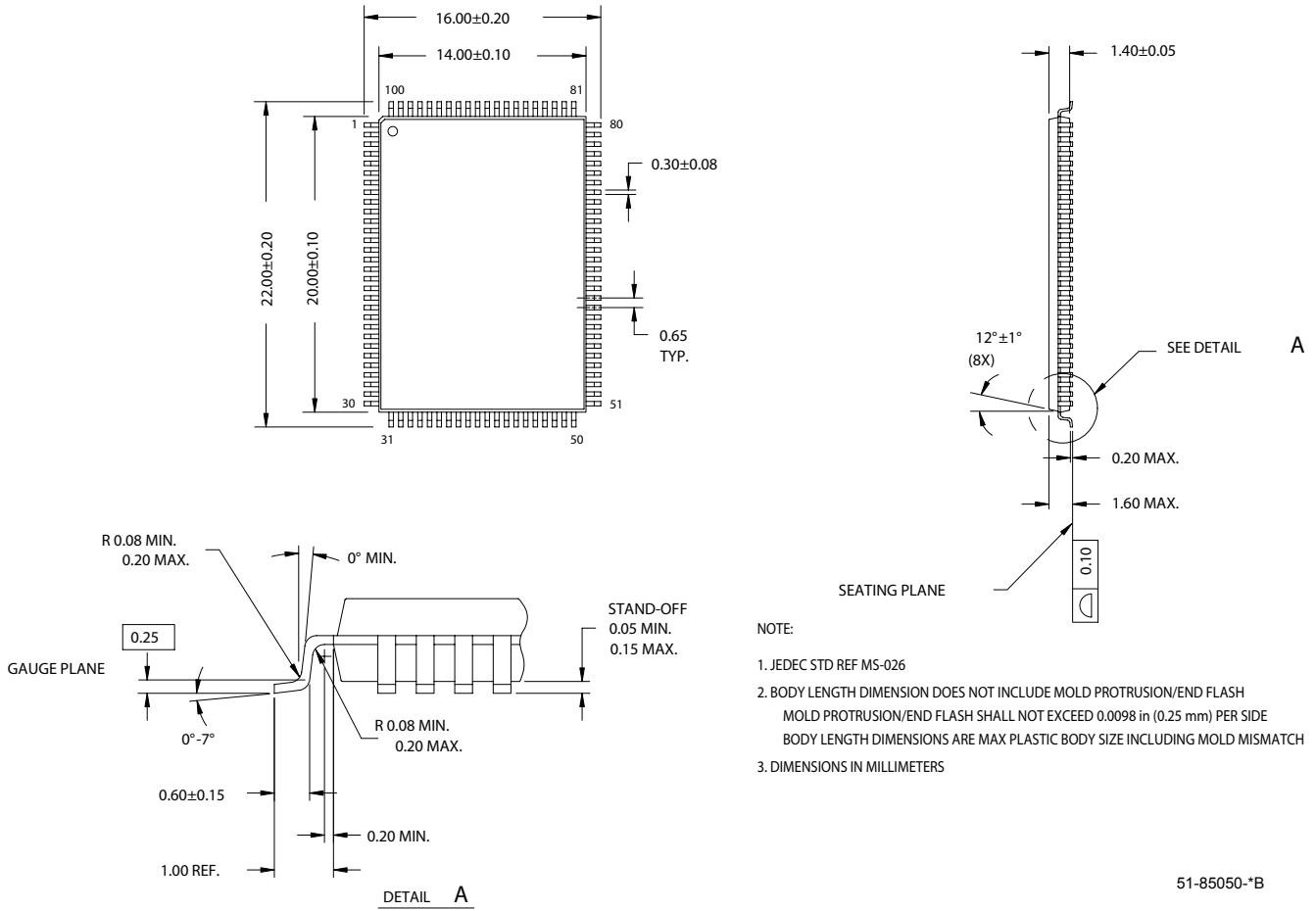
Not all of the speed, package and temperature ranges are available. Please contact your local sales representative or visit [www.cypress.com](http://www.cypress.com) for actual products offered.

Speed (MHz)	Ordering Code	Package Diagram	Part and Package Type	Operating Range	
133	CY7C1461AV33-133AXC	51-85050	100-Pin Thin Quad Flat Pack (14 x 20 x 1.4 mm) Pb-Free	Commercial	
	CY7C1463AV33-133AXC				
	CY7C1461AV33-133BZC	51-85165	165-Ball Fine-Pitch Ball Grid Array (15 x 17 x 1.4 mm)		
	CY7C1463AV33-133BZC				
	CY7C1461AV33-133BZXC	51-85165	165-Ball Fine-Pitch Ball Grid Array (15 x 17 x 1.4 mm) Pb-Free		
	CY7C1463AV33-133BZXC				
	CY7C1465AV33-133BGC	51-85167	209-Ball Fine-Pitch Ball Grid Array (14 x 22 x 1.76 mm)		
	CY7C1465AV33-133BGXC		209-Ball Fine-Pitch Ball Grid Array (14 x 22 x 1.76 mm) Pb-Free		
	CY7C1461AV33-133AXI	51-85050	100-Pin Thin Quad Flat Pack (14 x 20 x 1.4 mm) Pb-Free		Industrial
	CY7C1463AV33-133AXI				
	CY7C1461AV33-133BZI	51-85165	165-Ball Fine-Pitch Ball Grid Array (15 x 17 x 1.4 mm)		
	CY7C1463AV33-133BZI				
	CY7C1461AV33-133BZXI	51-85165	165-Ball Fine-Pitch Ball Grid Array (15 x 17 x 1.4 mm) Pb-Free		
	CY7C1463AV33-133BZXI				
CY7C1465AV33-133BGI	51-85167	209-Ball Fine-Pitch Ball Grid Array (14 x 22 x 1.76 mm)			
CY7C1465AV33-133BGXI		209-Ball Fine-Pitch Ball Grid Array (14 x 22 x 1.76 mm) Pb-Free			
100	CY7C1461AV33-100AXC	51-85050	100-Pin Thin Quad Flat Pack (14 x 20 x 1.4 mm) Pb-Free	Commercial	
	CY7C1463AV33-100AXC				
	CY7C1461AV33-100BZC	51-85165	165-Ball Fine-Pitch Ball Grid Array (15 x 17 x 1.4 mm)		
	CY7C1463AV33-100BZC				
	CY7C1461AV33-100BZXC	51-85165	165-Ball Fine-Pitch Ball Grid Array (15 x 17 x 1.4 mm) Pb-Free		
	CY7C1463AV33-100BZXC				
	CY7C1465AV33-100BGC	51-85167	209-Ball Fine-Pitch Ball Grid Array (14 x 22 x 1.76 mm)		
	CY7C1465AV33-100BGXC		209-Ball Fine-Pitch Ball Grid Array (14 x 22 x 1.76 mm) Pb-Free		
	CY7C1461AV33-100AXI	51-85050	100-Pin Thin Quad Flat Pack (14 x 20 x 1.4 mm) Pb-Free		Industrial
	CY7C1463AV33-100AXI				
	CY7C1461AV33-100BZI	51-85165	165-Ball Fine-Pitch Ball Grid Array (15 x 17 x 1.4 mm)		
	CY7C1463AV33-100BZI				
	CY7C1461AV33-100BZXI	51-85165	165-Ball Fine-Pitch Ball Grid Array (15 x 17 x 1.4 mm) Pb-Free		
	CY7C1463AV33-100BZXI				
CY7C1465AV33-100BGI	51-85167	209-Ball Fine-Pitch Ball Grid Array (14 x 22 x 1.76 mm)			
CY7C1465AV33-100BGXI		209-Ball Fine-Pitch Ball Grid Array (14 x 22 x 1.76 mm) Pb-Free			

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Package Diagrams

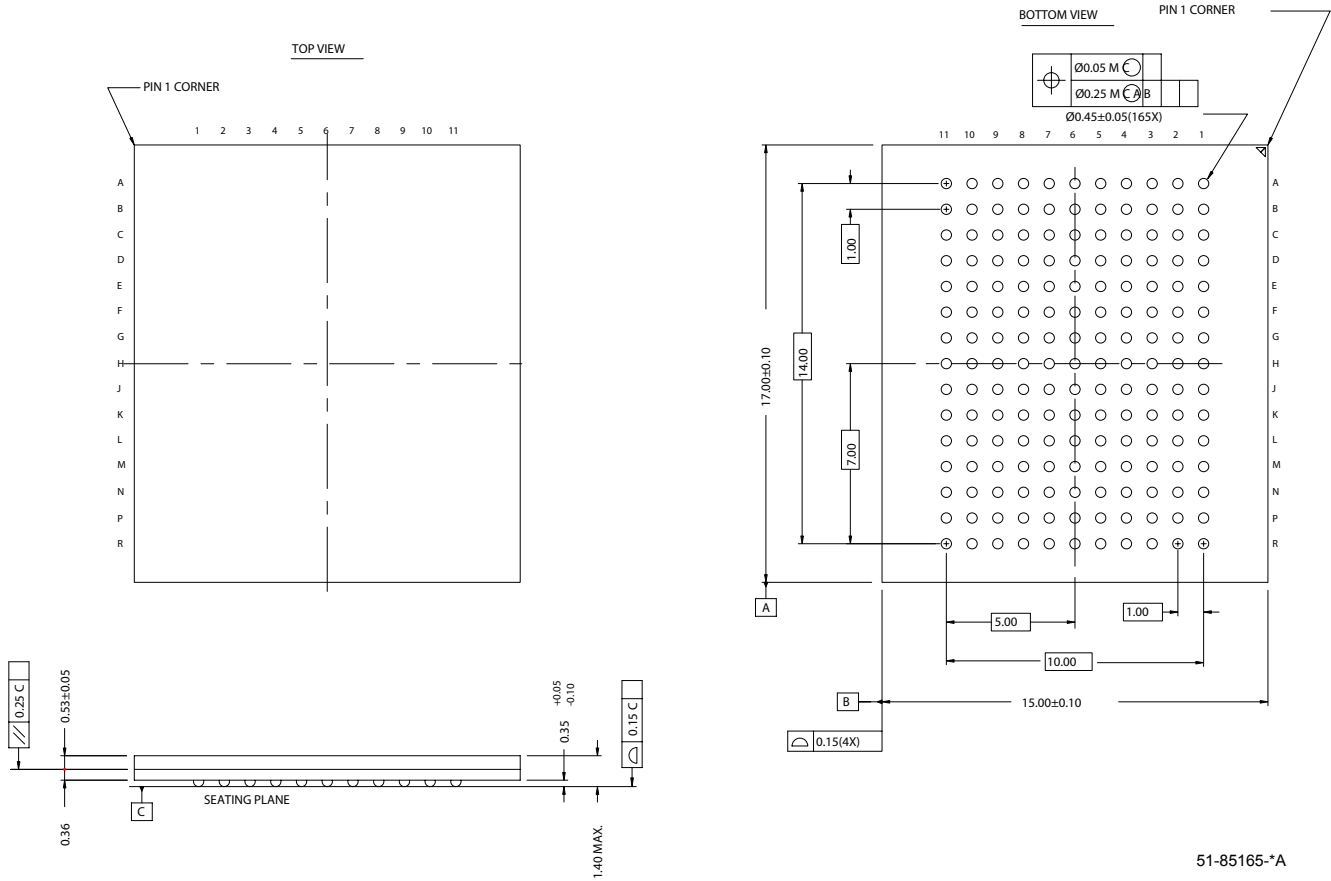
Figure 1. 100-Pin Thin Plastic Quad Flatpack (14 x 20 x 1.4 mm), 51-85050



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**Package Diagrams** (continued)

**Figure 2. 165-Ball FBGA (15 x 17 x 1.4 mm), 51-85165**

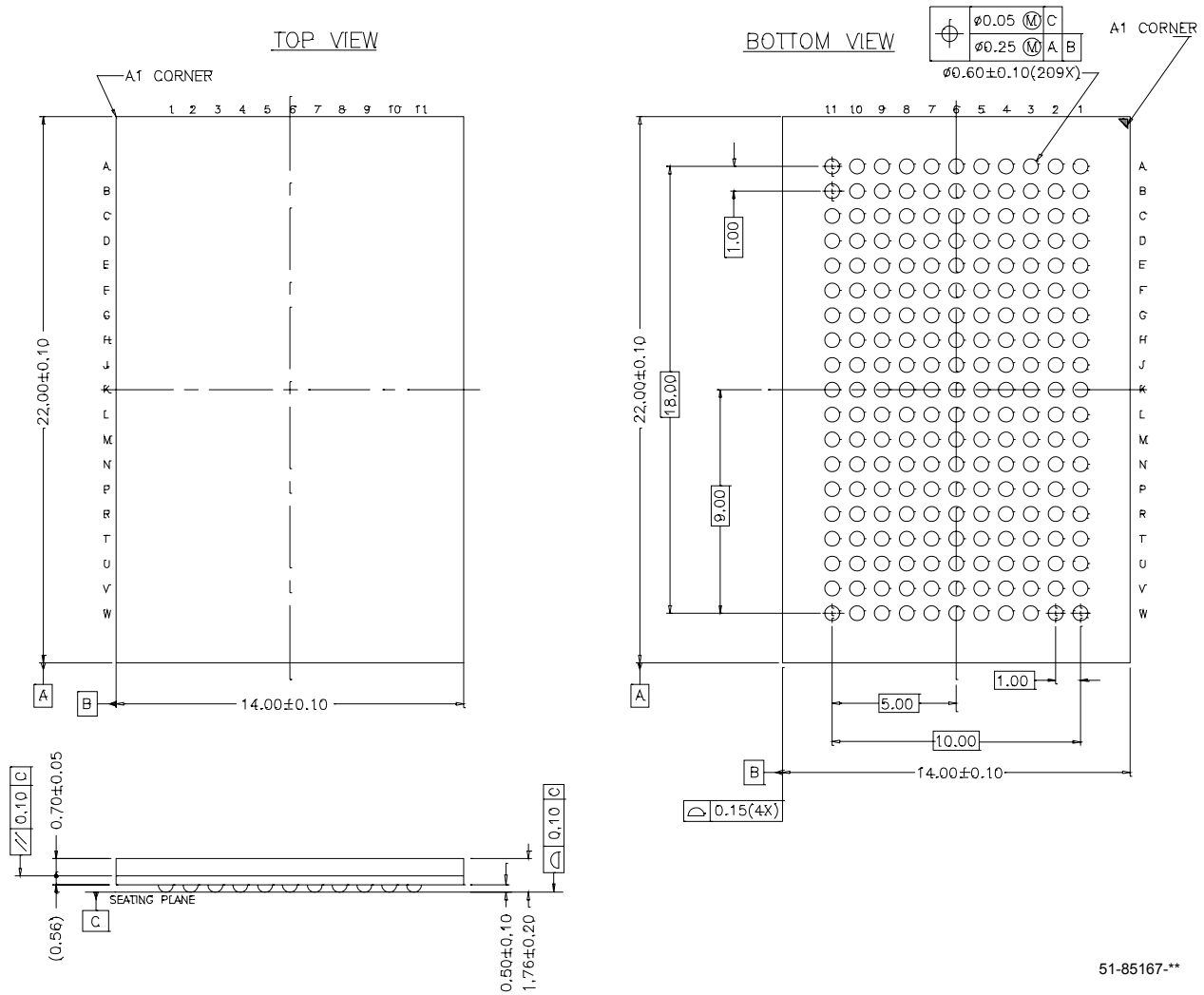


51-85165-A

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Package Diagrams (continued)

Figure 3. 209-Ball FBGA (14 x 22 x 1.76 mm), 51-85167



51-85167-\*\*

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**Document History Page**

Document Title: CY7C1461AV33/CY7C1463AV33/CY7C1465AV33 36-Mbit (1M x 36/2 M x 18/512K x 72) Flow-Through SRAM with NoBL™ Architecture Document Number: 38-05356				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	254911	See ECN	SYT	New data sheet Part number changed from previous revision. New and old part number differ by the letter "A"
*A	300131	See ECN	SYT	Removed 150- and 117-MHz Speed Bins Changed $\Theta_{JA}$ and $\Theta_{JC}$ from TBD to 25.21 and 2.58 °C/W, respectively, for TQFP package Added Pb-free information for 100-pin TQFP, 165 FBGA and 209 FBGA packages Added "Pb-free BG and BZ packages availability" below the Ordering Information
*B	320813	See ECN	SYT	Changed H9 pin from $V_{SSQ}$ to $V_{SS}$ on the Pin Configuration table for 209 FBGA Changed the test condition from $V_{DD} = \text{Min.}$ to $V_{DD} = \text{Max}$ for $V_{OL}$ in the Electrical Characteristics table Replaced the TBD's for $I_{DD}$ , $I_{SB1}$ , $I_{SB2}$ , $I_{SB3}$ and $I_{SB4}$ to their respective values Replaced TBD's for $\Theta_{JA}$ and $\Theta_{JC}$ to their respective values on the Thermal Resistance table for 165 FBGA and 209 FBGA Packages Changed $C_{IN}$ , $C_{CLK}$ and $C_{IO}$ to 6.5, 3 and 5.5 pF from 5, 5 and 7 pF for TQFP Package Removed "Pb-free BG packages availability" comment below the Ordering Information
*C	331551	See ECN	SYT	Modified Address Expansion balls in the pinouts for 165 FBGA and 209 FBGA Packages according to JEDEC standards and updated the Pin Definitions accordingly Modified $V_{OL}$ , $V_{OH}$ test conditions Replaced TBD to 100 mA for $I_{DDZZ}$ Changed $C_{IN}$ , $C_{CLK}$ and $C_{IO}$ to 7, 7 and 6 pF from 5, 5 and 7 pF for 165 FBGA Package Added Industrial Temperature Grade Changed $I_{SB2}$ and $I_{SB4}$ from 100 and 110 mA to 120 and 135 mA respectively Updated the Ordering Information by shading and unshading MPNs according to availability
*D	417547	See ECN	RXU	Converted from Preliminary to Final Changed address of Cypress Semiconductor Corporation on Page# 1 from "3901 North First Street" to "198 Champion Court" Changed $I_X$ current value in MODE from -5 & 30 $\mu\text{A}$ to -30 & 5 $\mu\text{A}$ respectively and also Changed $I_X$ current value in ZZ from -30 & 5 $\mu\text{A}$ to -5 & 30 $\mu\text{A}$ respectively on page# 20 Modified test condition from $V_{IH} \leq V_{DD}$ to $V_{IH} < V_{DD}$ Modified "Input Load" to "Input Leakage Current except ZZ and MODE" in the Electrical Characteristics Table Replaced Package Name column with Package Diagram in the Ordering Information table Replaced Package Diagram of 51-85050 from *A to *B Updated the Ordering Information
*E	473650	See ECN	VKN	Added the Maximum Rating for Supply Voltage on $V_{DDQ}$ Relative to GND. Changed $t_{TH}$ , $t_{TL}$ from 25 ns to 20 ns and $t_{DOV}$ from 5 ns to 10 ns in TAP AC Switching Characteristics table. Updated the Ordering Information table.
*F	1274733	See ECN	VKN/AESA	Corrected typo in the "NOP, STALL and DESELECT Cycles" waveform

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